CLAIMS

1. A synchronous mirror delay, comprising:

a ring oscillator operable to generate a plurality of tap clock signals with one tap clock signal being designated an oscillator clock signal, each tap clock signal having a respective delay relative to the oscillator clock signal;

a model delay line adapted to receive an input clock signal and operable to generate a model delayed clock signal in response to the input clock signal, the model delayed clock signal having a model delay relative to the input clock signal;

a coarse delay circuit adapted to receive the input clock signal and coupled to the ring oscillator and the model delay line, the coarse delay circuit operable to generate a coarse delay count responsive to the oscillator, input, and model delayed clock signals, and further operable to activate a coarse delay enable signal responsive to the delay count being equal to a reference count value;

a fine delay circuit coupled to the ring oscillator to receive the tap clock signals, coupled to the coarse delay circuit to receive the coarse delay enable signal, and adapted to receive the input clock signal, the fine delay circuit operable to latch the tap clock signals responsive to the input clock signal and to develop a fine delay from the latched tap clock signals, the fine delay circuit operable to activate a fine delay enable signal in response to the coarse delay enable signal, the fine delay enable signal having the fine delay relative to the coarse delay enable signal; and

an output circuit coupled to the coarse and fine delay circuits, the output circuit generating a delayed clock signal responsive to the coarse and fine delay enable signals going active.

2. The synchronous mirror delay of claim 1 wherein the coarse delay count initially has the reference count value, and wherein the coarse delay circuit is operable during an up-count mode responsive to a transition of the model delayed clock signal to increment the coarse delay count responsive to the oscillator clock signal, and the coarse delay circuit operable during a down-count mode responsive to a transition of the input clock

signal to decrement the coarse delay count responsive to the oscillator clock signal and to generate the coarse delay enable signal responsive to the coarse delay count being equal to the reference count value.

3. The synchronous mirror delay of claim 2 wherein the up-count mode is initiated responsive to a transition of the model delayed clock signal generated by the model delay line in response to an Nth transition of the input clock signal from a first logic level to a second logic level, and the down-count mode is initiated responsive to the N+1th transition of the input clock signal from the first to the second logic level.

4. The synchronous mirror delay of claim 1 wherein the fine delay circuit comprises:

a multiplexer having a plurality of inputs coupled to the ring oscillator, each input receiving a respective tap clock signal, the multiplexer operable to provide a respective tap clock signal on an output responsive to a plurality of input selection signals, with the tap clock signal on the output corresponding to the fine delay enable signal;

a latch and compare circuit coupled to the ring oscillator, the latch and compare circuit operable to latch the tap clock signals responsive to the input clock signal and to generate a plurality of fine delay signals responsive to the latched tap clock signals; and

a fine delay transform circuit coupled to receive the coarse delay enable signal and coupled to the latch and compare circuit and the multiplexer, the fine delay transform circuit operable in response to the fine delay signals to select a respective input selection signal and to activate the selected input selection signal responsive to the coarse delay enable signal going active.

5. The synchronous mirror delay of claim 4 wherein the multiplexer comprises a plurality of transmission gates.

6. The synchronous mirror delay of claim 4 wherein the ring oscillator includes N delay stages that generate tap clock signals T1-TN, respectively, and the latch and

compare circuit latches tap clock signals T1-TN from the ring oscillator and performs an XOR operation on each pair of latched tap clock signals T1-T2, T2-T3, and so on through TN-1-TN, and also performs an XOR operation on the pair T1 and TN, with each XOR operation generating a corresponding fine delay signal.

7. The synchronous mirror delay of claim 6 wherein the fine delay transform circuit operates in a first mode responsive to a selected one of the tap clock signals T1-TN having a first logic state.

8. The synchronous mirror delay of claim 7 wherein the fine delay transform circuit operates in a second mode responsive to a selected one of the tap clock signals T1-TN having a second logic state.

9. The synchronous mirror delay of claim 1 wherein the output circuit comprises an AND gate.

10. The synchronous mirror delay of claim 1 wherein the coarse delay circuit comprises:

an up/down counter coupled to receive the input clock signal and the model delayed clock signal, and coupled to the ring oscillator to receive the oscillator clock signal, the up/down counter operable responsive to a transition of the model delayed clock signal to increment the coarse delay count from the reference count value responsive to the oscillator clock signal, and operable responsive to a transition of the input clock signal to decrement the coarse delay count responsive to the oscillator clock signal; and

a comparator coupled to the up/down counter, the comparator activating the coarse delay enable signal responsive to the coarse delay count being equal to the reference count value.

11. A synchronous mirror delay, comprising:

an input buffer adapted to receive an input clock signal and operable to generate a buffered clock signal in response to the input clock signal;

a ring oscillator operable to generate a plurality of tap clock signals with one tap clock signal being designated an oscillator clock signal, each tap clock signal having a respective delay relative to the oscillator clock signal;

a model delay line coupled to the input buffer to receive the buffered clock signal and operable to generate a model delayed clock signal in response to the buffered clock signal, the model delayed clock signal having a model delay relative to the buffered clock signal;

a coarse delay circuit coupled to the input buffer, ring oscillator, and the model delay line, the coarse delay circuit operable to generate a coarse delay count responsive to the oscillator, buffered, and model delayed clock signals, and further operable to activate a coarse delay enable signal responsive to the delay count being equal to a reference count value;

a fine delay circuit coupled to the ring oscillator to receive the tap clock signals, coupled to the coarse delay circuit to receive the coarse delay enable signal, and coupled to the input buffer to receive the buffered clock signal, the fine delay circuit operable to latch the tap clock signals responsive to the buffered clock signal and to develop a fine delay from the latched tap clock signals, the fine delay circuit operable to activate a fine delay enable signal in response to the coarse delay enable signal, the fine delay enable signal having the fine delay relative to the coarse delay enable signal;

a delayed signal generation circuit coupled to the coarse and fine delay circuits and operable to generate a delayed clock signal responsive to the coarse and fine delay enable signals going active; and

an output buffer coupled to the delayed signal generation circuit and operable to generate a synchronized clock signal responsive to the delayed clock signal, the synchronized clock signal having edges that are synchronized with edges of the input clock signal.

12. The synchronous mirror delay of claim 11 wherein the coarse delay count initially has the reference count value, and wherein the coarse delay circuit is operable during an up-count mode responsive to a transition of the model delayed clock signal to increment the coarse delay count responsive to the oscillator clock signal, and the coarse delay circuit operable during a down-count mode responsive to a transition of the buffered clock signal to decrement the coarse delay count responsive to the oscillator clock signal and to generate the coarse delay enable signal responsive to the coarse delay count being equal to the reference count value.

13. The synchronous mirror delay of claim 12 wherein the up-count mode is initiated responsive to a transition of the model delayed clock signal generated by the model delay line in response to an Nth transition of the buffered clock signal from a first logic level to a second logic level, and the down-count mode is initiated responsive to the N+1th transition of the buffered clock signal from the first to the second logic level.

14. The synchronous mirror delay of claim 11 wherein the fine delay circuit comprises:

a multiplexer having a plurality of inputs coupled to the ring oscillator, each input receiving a respective tap clock signal, the multiplexer operable to provide a respective tap clock signal on an output responsive to a plurality of input selection signals, with the tap clock signal on the output corresponding to the fine delay enable signal;

a latch and compare circuit coupled to the ring oscillator, the latch and compare circuit operable to latch the tap clock signals responsive to the buffered clock signal and to generate a plurality of fine delay signals responsive to the latched tap clock signals; and

a fine delay transform circuit coupled to receive the coarse delay enable signal and coupled to the latch and compare circuit and the multiplexer, the fine delay transform circuit operable in response to the fine delay signals to select a respective input selection signal and to activate the selected input selection signal responsive to the coarse delay enable signal going active.

15. The synchronous mirror delay of claim 14 wherein the multiplexer comprises a plurality of transmission gates.

16. The synchronous mirror delay of claim 14 wherein the ring oscillator includes N delay stages that generate tap clock signals T1-TN, respectively, and the latch and compare circuit latches tap clock signals T1-TN from the ring oscillator and performs an XOR operation on each pair of latched tap clock signals T1-T2, T2-T3, and so on through TN-1-TN, and also performs an XOR operation on the pair T1 and TN, with each XOR operation generating a corresponding fine delay signal.

17. The synchronous mirror delay of claim 16 wherein the fine delay transform circuit operates in a first mode responsive to a selected one of the tap clock signals T1-TN having a first logic state.

18. The synchronous mirror delay of claim 17 wherein the fine delay transform circuit operates in a second mode responsive to a selected one of the tap clock signals T1-TN having a second logic state.

19. The synchronous mirror delay of claim 11 wherein the input buffer introduces a delay D1 to the buffered clock signal relative to the input clock signal and the output buffer introduces a delay D2 to the synchronized clock signal relative to the delayed clock signal, and the model delay as first and second components that model the delays D1 and D2.

20. The synchronous mirror delay of claim 11 wherein the coarse delay circuit comprises:

an up/down counter coupled to receive the buffered clock signal and the model delayed clock signal, and coupled to the ring oscillator to receive the oscillator clock signal, the up/down counter operable responsive to a transition of the model delayed clock signal to increment the coarse delay count from the reference count value responsive to

the oscillator clock signal, and operable responsive to a transition of the buffered clock signal to decrement the coarse delay count responsive to the oscillator clock signal; and

a comparator coupled to the up/down counter, the comparator activating the coarse delay enable signal responsive to the coarse delay count being equal to the reference count value.

21. A synchronous mirror delay, comprising:

a first input buffer adapted to receive an input clock signal and operable to generate a buffered clock signal in response to the input clock signal;

a first ring oscillator operable to generate a plurality of tap clock signals with one tap clock signal being designated an oscillator clock signal, each tap clock signal having a respective delay relative to the oscillator clock signal;

a first model delay line coupled to the first input buffer to receive the buffered clock signal and operable to generate a model delayed clock signal in response to the buffered clock signal, the model delayed clock signal having a model delay relative to the buffered clock signal;

a first rising-edge synchronous mirror delay circuit coupled to the first ring oscillator and operable to generate a delayed clock signal have course and fine delays developed from the tap clock signals, the coarse and fine delays defining a delay of the delayed clock signal relative to even rising edges of the input clock signal;

a second rising-edge synchronous mirror delay circuit coupled to the first ring oscillator and operable to generate a delayed clock signal have course and fine delays developed from the tap clock signals, the coarse and fine delays defining a delay of the delayed clock signal relative to odd rising edges of the input clock signal;

a second input buffer adapted to receive an input clock signal and operable to generate a buffered clock signal in response to the input clock signal;

a second ring oscillator operable to generate a plurality of tap clock signals with one tap clock signal being designated an oscillator clock signal, each tap clock signal having a respective delay relative to the oscillator clock signal;

a model delay line coupled to the second input buffer to receive the buffered clock signal and operable to generate a model delayed clock signal in response to the buffered clock signal, the model delayed clock signal having a model delay relative to the buffered clock signal;

a first falling-edge synchronous mirror delay circuit coupled to the second ring oscillator and operable to generate a delayed clock signal have course and fine delays developed from the tap clock signals, the coarse and fine delays defining a delay of the delayed clock signal relative to even falling edges of the input clock signal;

a second falling-edge synchronous mirror delay circuit coupled to the ring oscillator and operable to generate a delayed clock signal have course and fine delays developed from the tap clock signals, the coarse and fine delays defining a delay of the delayed clock signal relative to odd falling edges of the input clock signal; and

an output circuit coupled to the first and second rising- and falling-edge synchronous mirror delay circuits, and operable to develop a synchronized clock signal responsive to the delayed clock signals from the mirror delay circuits, the synchronized clock signal being synchronized with the input clock signal.

22. The synchronous mirror delay of claim 21 wherein each of the synchronous mirror delay circuits includes a fine delay circuit, comprising:

a multiplexer having a plurality of inputs coupled to the ring oscillator, each input receiving a respective tap clock signal, the multiplexer operable to provide a respective tap clock signal on an output responsive to a plurality of input selection signals, with the tap clock signal on the output corresponding to the fine delay enable signal;

a latch and compare circuit coupled to the ring oscillator, the latch and compare circuit operable to latch the tap clock signals responsive to the input clock signal and to generate a plurality of fine delay signals responsive to the latched tap clock signals; and

a fine delay transform circuit coupled to receive the coarse delay enable signal and coupled to the latch and compare circuit and the multiplexer, the fine delay transform circuit operable in response to the fine delay signals to select a respective input

selection signal and to activate the selected input selection signal responsive to the coarse delay enable signal going active.

23. The synchronous mirror delay of claim 22 wherein the multiplexer comprises a plurality of transmission gates.

24. The synchronous mirror delay of claim 21 wherein each ring oscillator includes N delay stages that generate tap clock signals T1-TN, respectively, and the latch and compare circuit latches tap clock signals T1-TN from the ring oscillator and performs an XOR operation on each pair of latched tap clock signals T1-T2, T2-T3, and so on through TN-1-TN, and also performs an XOR operation on the pair T1 and TN, with each XOR operation generating a corresponding fine delay signal.

25. The synchronous mirror delay of claim 21 wherein the output circuit comprises a first OR gate coupled to receive the delayed clock signals from the first and second rising-edge synchronous mirror delay circuits, a second OR gate coupled to receive the delayed clock signals from the first and second falling-edge synchronous mirror delay circuits, an RS flip-flop coupled to the first and second OR gates to receive set and reset inputs and operable to develop an output delayed clock signal responsive to the reset and set inputs, and an output buffer coupled to the RS flip-flop and operable to generate the synchronized clock signal responsive to the output delayed clock signal.

26. The synchronous mirror delay of claim 21 wherein each synchronous mirror delay circuit includes a coarse delay circuit, comprising:

an up/down counter coupled to receive the input clock signal and the model delayed clock signal, and coupled to the ring oscillator to receive the oscillator clock signal, the up/down counter operable responsive to a transition of the model delayed clock signal to increment the coarse delay count from the reference count value responsive to the oscillator clock signal, and operable responsive to a transition of the input clock signal to decrement the coarse delay count responsive to the oscillator clock signal; and

a comparator coupled to the up/down counter, the comparator activating the coarse delay enable signal responsive to the coarse delay count being equal to the reference count value.

27. A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

a synchronous mirror delay coupled to at least the control circuit and adapted to receive an input clock signal, the synchronous mirror delay operable to generate a delayed clock signal and the control circuit generating control signals in response to the delayed clock signal, the synchronous mirror delay comprising,

a ring oscillator operable to generate a plurality of tap clock signals with one tap clock signal being designated an oscillator clock signal, each tap clock signal having a respective delay relative to the oscillator clock signal;

a model delay line adapted to receive an input clock signal and operable to generate a model delayed clock signal in response to the input clock signal, the model delayed clock signal having a model delay relative to the input clock signal;

a coarse delay circuit adapted to receive the input clock signal and coupled to the ring oscillator and the model delay line, the coarse delay circuit operable to generate a coarse delay count responsive to the oscillator, input, and model delayed clock signals, and further operable to activate a coarse delay enable signal responsive to the delay count being equal to a reference count value;

a fine delay circuit coupled to the ring oscillator to receive the tap clock signals, coupled to the coarse delay circuit to receive the coarse delay enable signal,

and adapted to receive the input clock signal, the fine delay circuit operable to latch the tap clock signals responsive to the input clock signal and to develop a fine delay from the latched tap clock signals, the fine delay circuit operable to activate a fine delay enable signal in response to the coarse delay enable signal, the fine delay enable signal having the fine delay relative to the coarse delay enable signal; and

an output circuit coupled to the coarse and fine delay circuits, the output circuit generating a delayed clock signal responsive to the coarse and fine delay enable signals going active.

28. The memory device of claim 27 wherein the memory device comprises a DDR SDRAM and the synchronous mirror delay receives complementary input clock signals and generates the delayed clock signal that is synchronized to the rising and falling edges of the clock signals, the delayed clock signal being applied to clock an output driver coupled to the data bus.

29. A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, comprising,

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

a synchronous mirror delay coupled to at least the control circuit and adapted to receive an input clock signal, the synchronous mirror delay operable to

generate a delayed clock signal and the control circuit generating control signals in response to the delayed clock signal, the synchronous mirror delay comprising,

a ring oscillator operable to generate a plurality of tap clock signals with one tap clock signal being designated an oscillator clock signal, each tap clock signal having a respective delay relative to the oscillator clock signal;

a model delay line adapted to receive an input clock signal and operable to generate a model delayed clock signal in response to the input clock signal, the model delayed clock signal having a model delay relative to the input clock signal;

a coarse delay circuit adapted to receive the input clock signal and coupled to the ring oscillator and the model delay line, the coarse delay circuit operable to generate a coarse delay count responsive to the oscillator, input, and model delayed clock signals, and further operable to activate a coarse delay enable signal responsive to the delay count being equal to a reference count value;

a fine delay circuit coupled to the ring oscillator to receive the tap clock signals, coupled to the coarse delay circuit to receive the coarse delay enable signal, and adapted to receive the input clock signal, the fine delay circuit operable to latch the tap clock signals responsive to the input clock signal and to develop a fine delay from the latched tap clock signals, the fine delay circuit operable to activate a fine delay enable signal in response to the coarse delay enable signal, the fine delay enable signal having the fine delay relative to the coarse delay enable signal; and

an output circuit coupled to the coarse and fine delay circuits, the output circuit generating a delayed clock signal responsive to the coarse and fine delay enable signals going active.

30. The computer system of claim 29 wherein the memory device comprises a DDR SDRAM and the synchronous mirror delay receives complementary input clock signals and generates the delayed clock signal that is synchronized to the rising and falling edges of the clock signals, the delayed clock signal being applied to clock an output driver coupled to the data bus.

31. A method for generating a delayed clock signal having a delay relative to an applied clock signal, the method comprising:

generating a plurality of oscillator clock signals, each oscillator clock signal having a frequency that is greater than the applied clock signal, with one oscillator clock signal being designated a reference oscillator clock signal and each oscillator clock signal having a delay relative to the reference oscillator clock signal;

generating a model delayed clock signal in response to the applied clock signal, the model delayed clock signal having a model delay relative to the applied clock signal;

initiating a time-to-digital count coarse delay interval in response to a transition of the model delayed clock signal generated in response to an Nth transition of the applied clock signal;

incrementing a course delay count responsive to the reference oscillator clock signal during the first coarse delay interval;

terminating the first coarse delay interval responsive to an N+1th transition of the applied clock signal;

storing the states of the oscillator clock signals when the first coarse delay interval is terminated;

initiating a digital-to-time coarse delay interval in response to the applied clock signal;

decrementing the coarse delay count responsive to the reference oscillator clock signal during the digital-to-time coarse delay interval;

calculating a digital-to-time fine delay from the stored states of the oscillator clock signals; and

generating the delayed clock signal having the delay relative to the applied clock signal that is determined by the coarse delay count being equal to a reference value plus the calculated digital-to-fine delay.

32. The method of claim 31 wherein calculating a digital-to-time fine delay from the stored states of the oscillator clock signals comprises calculating the fine delay in a

according to a first methodology responsive to a selected one of the tap clock signals T1-TN having a first logic state.

33. The method of claim 32 wherein calculating a digital-to-time fine delay from the stored states of the oscillator clock signals comprises calculating the fine delay according to a second methodology responsive to a selected one of the tap clock signals T1-TN having a second logic state.

34. The method of claim 31 wherein storing the states of the oscillator clock signals when the first coarse delay interval is terminated comprises storing the instantaneous states of the clock signals, and thereafter performing an XOR operation on adjacent pairs of clock signals to generate a plurality of fine delay control signals, with the fine delay control signal having a false value indicating the location of the reference oscillator clock signal edge at the point in time when the first coarse delay interval is terminated.

35. A method for generating a delayed clock signal having a delay relative to an applied clock signal, the method comprising:

generating a plurality of oscillator clock signals, each oscillator clock signal having a frequency that is greater than the applied clock signal, with one oscillator clock signal being designated a reference oscillator clock signal and each oscillator clock signal having a delay relative to the reference oscillator clock signal;

timing a coarse delay time in response to transitions of the reference oscillator clock signal;

storing the state of the oscillator clock signals at a first time;

replaying the coarse delay time;

calculating a fine delay time from the states of the oscillator clock signals at the first time; and

generating the delayed clock signal having a delay relative to the applied clock signal that is given by the sum of the coarse delay time plus the replayed coarse delay time plus the fine delay time.

36. The method of claim 35 wherein replaying the coarse delay time comprises timing a digital-to-time coarse delay time in response to transitions of the reference oscillator clock signal after the first time.

37. The method of claim 35 wherein storing the state of the oscillator clock signals at a first time comprises storing the instantaneous states of the oscillator clock signals, and thereafter performing an XOR operation on adjacent pairs of clock signals to generate a plurality of fine delay control signals, with the fine delay control signal having a false value indicating the location of the reference oscillator clock signal edge at the first time.

38. The method of claim 35 wherein a first circuit generates the plurality of oscillator clocks signals, times the coarse delay time, and calculates the fine delay time, and wherein a second circuit replays the coarse delay time and generates the delayed clock signal.

39. The method of claim 38 wherein the first and second circuits are different circuits.

40. A digital measuring system comprising:

a ring oscillator with a start function, operable to generate a plurality of tap clock signals with one tap clock signal being designated an oscillator clock signal, each tap clock signal having a respective delay relative to the oscillator clock signal;

a coarse delay measuring circuit adapted to receive the ring oscillator start signal and a measure signal, and coupled to the ring oscillator clock signal, operable to generate a cycle count of the oscillator clock signal between the start signal and the measure signal and thereby to develop a coarse digital delay measurement result;

a fine delay measuring circuit coupled to the ring oscillator to receive the tap clock signals and adapted to receive the measure signal operable to latch the tap clock signals responsive to the measure signal and thereby to develop a fine digital delay measurement result.

41. A digital replay system comprising:

a ring oscillator with a start function, operable to generate a plurality of tap clock signals with one tap clock signal being designated an oscillator clock signal, each tap clock signal having a respective delay relative to the oscillator clock signal;

a coarse delay replay circuit adapted to receive and store coarse digital delay measurement data from the digital delay measuring system and the ring oscillator start signal, and coupled to the ring oscillator clock signal, operable to generate a cycle count based on the oscillator clock signal and to generate a coarse delay replay signal when the cycle count equals the stored digital delay measurement data;

a fine delay replay circuit to receive the fine digital delay measurement data and the coarse delay replay signal, and coupled to the ring oscillator to receive the tap clock signals, and adapted to develop a fine delay replay signal at the first digitally selected tap clock edge after the activation of the coarse delay replay signal.